Claims:

What is claimed is:

1. A loop filter for a phase locked loop ("PLL") circuit which locks a frequency of a signal to a reference frequency, comprising:

a proportional path circuit which receives a charge pump output and determines and holds a charge to be directed to or taken from a PLL circuit throughout an update period based on a detected phase difference for the update period for locking a frequency of a signal for the PLL circuit to a reference frequency; and

an integral path circuit coupled to the proportional path circuit wherein the integral path circuit receives another charge pump output and tracks a total charge level for the PLL circuit based on phase differences for present and prior update periods.

2. The loop filter according to Claim 1, wherein the charge pump output is from one charge pump and the another charge pump output is from another charge pump.

3. The loop filter according to Claim 1, wherein the charge pump output is a predetermined scaled charge output and the another charge pump output is another predetermined scaled charge output wherein the predetermined scaled charge output and the another predetermined scaled charge output are both from a single charge pump.

4. The loop filter according to Claim 2, wherein the proportional path circuit further comprises:

a transconductance stage, which receives as an input the charge pump output, for converting a voltage signal based on the signal to a current signal;

a capacitor that is able to couple to the charge pump output of the one charge pump or to a reset voltage level wherein the capacitor is respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level; and

another capacitor that is able to couple to the charge pump output of the one charge pump or to the reset voltage level wherein the another capacitor is also respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level.

5. The loop filter according to Claim 4, wherein the proportional path circuit further comprises:

a hold switch activated to couple the capacitor to the one charge pump;

a reset switch activated to couple the capacitor to a reset voltage source to set the capacitor to the reset voltage level;

another hold switch activated to couple the another capacitor to the one charge pump; and

another reset switch activated to couple the another capacitor to the reset voltage source to set the another capacitor to the reset voltage level.

6. The loop filter according to Claim 5, wherein the detected phase difference is detected by a phase frequency detector and wherein the phase frequency detector controls activation and deactivation of the hold switch, the reset switch, the another hold switch, and the another reset switch to charge, hold, and reset the capacitor and the another capacitor at appropriate times.

7. The loop filter according to Claim 6, wherein the charge of the capacitor is reset and wherein:

the phase frequency detector detects a beginning edge of the phase difference and deactivates the hold switch and the reset switch to couple the capacitor to the one charge pump to set the capacitor with the charge;

the phase frequency detector then detects a finishing edge of the phase difference and activates the hold switch to hold the capacitor with the charge and maintains the reset switch as deactivated so that the capacitor is coupled between the input of the transconductance stage and ground and further deactivates the another hold switch and activates the another reset switch to couple the another capacitor to the reset voltage source to set the another capacitor to the reset voltage level and to uncouple the another capacitor from the one charge pump; and

the phase frequency detector maintains the charge of the capacitor until the phase frequency detector detects a next phase difference.

8. The loop filter according to Claim 7, wherein:

the phase frequency detector detects a beginning edge of the next phase difference and maintains the another hold switch as deactivated and deactivates the another reset switch to couple the another capacitor to the one charge pump to set the another capacitor with the charge;

the phase frequency detector then detects a finishing edge of the next phase difference and activates the another hold switch to hold the another capacitor with the charge and maintains the another reset switch as deactivated so that the another capacitor is coupled between the input of the transconductance stage and ground and further deactivates the hold switch and activates the reset switch to couple the capacitor to the reset voltage source to set the capacitor to the reset voltage level and to uncouple the capacitor from the one charge pump; and

the phase frequency detector maintains the charge of the another capacitor until the phase frequency detector detects a following phase difference.

9. The loop filter according to Claim 8, wherein the phase frequency detector repeats the charging, holding, and resetting of the capacitor and the another capacitor for future phase differences detected by the phase frequency detector.

10. A method for implementing a loop filter for a phase locked loop ("PLL") circuit which locks a frequency of a signal to a reference frequency, comprising:

receiving, by a proportional path circuit, a charge pump output and determining and holding, by the proportional path circuit, a charge to be directed to or taken from a PLL circuit throughout an update period based on a detected phase difference for the update period for locking a frequency of a signal for the PLL circuit to a reference frequency; and

receiving, by an integral path circuit coupled to the proportional path circuit, another charge pump output and tracking, by the integral path circuit, a total charge level for the PLL circuit based on phase differences for present and prior update periods.

11. The method according to Claim 10, wherein:

the receiving by a proportional path circuit step further comprises the step of receiving the charge pump output from one charge pump, and

the receiving by an integral path circuit step further comprises the step of receiving the another charge pump output from another charge pump.

12. The method according to Claim 10, wherein:

the receiving by a proportional path circuit step further comprises the step of receiving the charge pump output as a predetermined scaled charge output, and

the receiving by an integral path circuit step further comprises the step of receiving the another charge pump output as another predetermined scaled charge output, and

wherein the predetermined scaled charge output and the another predetermined scaled charge output are both from a single charge pump.

13. The method according to Claim 11, further comprising the steps of:

receiving as an input, by a transconductance stage of the proportional path circuit, the charge pump output for converting a voltage signal based on the signal to a current signal;

coupling a capacitor to the charge pump output of the one charge pump or to a reset voltage level wherein the capacitor is respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level; and

coupling another capacitor to the charge pump output of the one charge pump or to the reset voltage level wherein the another capacitor is also respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level.

14. The method according to Claim 13, further comprising the steps of:

activating a hold switch to couple the capacitor to the one charge pump;

activating a reset switch to couple the capacitor to a reset voltage source to set the capacitor to the reset voltage level;

activating another hold switch to couple the another capacitor to the one charge pump; and

activating another reset switch to couple the another capacitor to the reset voltage source to set the another capacitor to the reset voltage level.

15. The method according to Claim 14, further comprising the steps of:

detecting, by a phase frequency detector, the detected phase difference, and

controlling, by the phase frequency detector, activation and deactivation of the hold switch, the reset switch, the another hold switch, and the another reset switch to charge, hold, and reset the capacitor and the another capacitor at appropriate times.

16. The method according to Claim 15, further comprising the steps of:

resetting the charge of the capacitor;

detecting, by the phase frequency detector, a beginning edge of the phase difference and deactivating, by the phase frequency detector, the hold switch and the reset switch to couple the capacitor to the one charge pump to set the capacitor with the charge;

detecting, by the phase frequency detector, a finishing edge of the phase difference and activating, by the phase frequency detector, the hold switch to hold the capacitor with the charge and maintaining, by the phase frequency detector, the reset switch as deactivated so that the capacitor is coupled between the input of the transconductance stage and ground and further deactivating, by the phase frequency detector, the another hold switch, and activating, by the phase frequency detector, the another reset switch to couple the another capacitor to the reset voltage source to set the another capacitor to the reset voltage level and to uncouple the another capacitor from the one charge pump; and

maintaining, by the phase frequency detector, the charge of the capacitor until the phase frequency detector detects a next phase difference.

17. The method according to Claim 16, further comprising the steps of:

detecting, by the phase frequency detector, a beginning edge of the next phase difference and maintaining, by the phase frequency detector, the another hold switch as deactivated and deactivating, by the phase frequency detector, the another reset switch to couple the another capacitor to the one charge pump to set the another capacitor with the charge;

detecting, by the phase frequency detector, a finishing edge of the next phase difference and activating, by the phase frequency detector, the another hold switch to hold the another capacitor with the charge and maintaining, by the phase frequency detector, the another reset switch as deactivated so that the another capacitor is coupled between the input of the transconductance stage and ground and further deactivating, by the phase frequency detector, the hold switch and activating, by the phase frequency detector, the reset switch to couple the capacitor to the reset voltage source to set the capacitor to the reset voltage level and to uncouple the capacitor from the one charge pump; and

maintaining, by the phase frequency detector, the charge of the another capacitor until the phase frequency detector detects a following phase difference.

18. The method according to Claim 17, further comprising the step of:

repeating, by the phase frequency detector, the operations of charging, holding, and resetting of the capacitor and the another capacitor for future phase differences detected by the phase frequency detector.

19. A phase-locked loop circuit for locking a frequency of a signal to a reference frequency, comprising:

a phase frequency detector, a loop filter, a current adder, and a current-controlled oscillator coupled together in series wherein the phase frequency detector receives as an input a signal having a reference frequency and wherein an output of the current-controlled oscillator is fed back and received as another input by the phase frequency detector; and

wherein the loop filter further comprises:

a proportional path circuit which receives a charge pump output and determines and holds a charge to be directed to or taken from the phase-locked loop circuit throughout an update period based on a detected phase difference for the update period for locking a frequency of a signal for the phase-locked loop circuit to the reference frequency; and

an integral path circuit coupled to the proportional path circuit wherein the integral path circuit receives another charge pump output and tracks a total charge level for the phase-locked loop circuit based on phase differences for present and prior update periods.

20. The phase-locked loop circuit according to Claim 19, wherein the charge pump output is from one charge pump and the another charge pump output is from another charge pump.

21. The phase-locked loop circuit according to Claim 19, wherein the charge pump output is a predetermined scaled charge output and the another charge pump output is another predetermined scaled charge output wherein the predetermined scaled charge output and the another predetermined scaled charge output are both from a single charge pump.

22. The phase-locked loop circuit according to Claim 20, wherein the proportional path circuit further comprises:

a transconductance stage, which receives as an input the charge pump output, for converting a voltage signal based on the signal to a current signal;

a capacitor that is able to couple to the charge pump output of the one charge pump or to a reset voltage level wherein the capacitor is respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level; and

another capacitor that is able to couple to the charge pump output of the one charge pump or to the reset voltage level wherein the another capacitor is also respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level.

23. The phase-locked loop circuit according to Claim 22, wherein the proportional path circuit further comprises:

a hold switch activated to couple the capacitor to the one charge pump;

a reset switch activated to couple the capacitor to a reset voltage source to set the capacitor to the reset voltage level;

another hold switch activated to couple the another capacitor to the one charge pump; and

another reset switch activated to couple the another capacitor to the reset voltage source to set the another capacitor to the reset voltage level.

24. The phase-locked loop circuit according to Claim 23, wherein the detected phase difference is detected by a phase frequency detector and wherein the phase frequency detector controls activation and deactivation of the hold switch, the reset switch, the another hold switch, and the another reset switch to charge, hold, and reset the capacitor and the another capacitor at appropriate times.

25. The phase-locked loop circuit according to Claim 19, further comprising:

an N divider coupled to the input of the phase frequency detector to divide the input by an N factor wherein the N-divided input is directed into the phase frequency detector; and

an M divider coupled to the output of the current controlled oscillator wherein the M-divided output is fed back to the phase frequency detector.

26. A method for operating and implementing a phase-locked loop circuit for locking a frequency of a signal to a reference frequency, comprising:

coupling together in series a phase frequency detector, a loop filter, a current adder, and a current-controlled oscillator;

receiving as an input, by the phase frequency detector, a signal having a reference frequency;

feeding back and receiving, by the phase frequency detector, an output of the current-controlled oscillator; and

implementing and operating the loop filter by:

receiving, by a proportional path circuit, a charge pump output from one charge pump;

determining and holding, by the proportional path circuit, a charge to be directed to or taken from the phase-locked loop circuit throughout an update period based on a detected phase difference by the phase difference for the update period for locking a frequency of the signal to the reference frequency;

coupling an integral path circuit to the proportional path circuit;

receiving, by the integral path circuit, another charge pump output from another charge pump; and

tracking, by the integral path circuit, a total charge level for the phase-locked loop circuit based on phase differences for present and prior update periods.

27. The method according to Claim 26, further comprising the steps of:

receiving as an input, by a transconductance stage, the charge pump output for converting a voltage signal based on the signal to a current signal;

coupling a capacitor to the charge pump output of the one charge pump or to a reset voltage level wherein the capacitor is respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level;

coupling another capacitor to the charge pump output of the one charge pump or to the reset voltage level wherein the another capacitor is also respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level;

activating a hold switch to couple the capacitor to the one charge pump;

activating a reset switch to couple the capacitor to a reset voltage source to set the capacitor to the reset voltage level;

activating another hold switch to couple the another capacitor to the one charge pump; and

activating another reset switch to couple the another capacitor to the reset voltage source to set the another capacitor to the reset voltage level.

28. The method according to Claim 27, further comprising the steps of:

resetting the charge of the capacitor;

detecting, by the phase frequency detector, a beginning edge of the phase difference and deactivating, by the phase frequency detector, the hold switch and the reset switch to couple the capacitor to the one charge pump to set the capacitor with the charge;

detecting, by the phase frequency detector, a finishing edge of the phase difference and activating, by the phase frequency detector, the hold switch to hold

the capacitor with the charge and maintaining, by the phase frequency detector, the reset switch as deactivated so that the capacitor is coupled between the input of the transconductance stage and ground and further deactivating, by the phase frequency detector, the another hold switch, and activating, by the phase frequency detector, the another reset switch to couple the another capacitor to the reset voltage source to set the another capacitor to the reset voltage level and to uncouple the another capacitor from the one charge pump; and

maintaining, by the phase frequency detector, the charge of the capacitor until the phase frequency detector detects a next phase difference.

29. The method according to Claim 28, further comprising the steps of:

detecting, by the phase frequency detector, a beginning edge of the next phase difference and maintaining, by the phase frequency detector, the another hold switch as deactivated and deactivating, by the phase frequency detector, the another reset switch to couple the another capacitor to the one charge pump to set the another capacitor with the charge;

detecting, by the phase frequency detector, a finishing edge of the next phase difference and activating, by the phase frequency detector, the another hold switch to hold the another capacitor with the charge and maintaining, by the phase frequency detector, the another reset switch as deactivated so that the another capacitor is coupled between the input of the transconductance stage and ground and further deactivating, by the phase frequency detector, the hold switch and activating, by the phase frequency detector, the reset switch to couple the capacitor to the reset voltage source to set the capacitor to the reset voltage level and to uncouple the capacitor from the one charge pump; and

maintaining, by the phase frequency detector, the charge of the another capacitor until the phase frequency detector detects a following phase difference.

30. The method according to Claim 29, further comprising the step of:

repeating, by the phase frequency detector, the operations of charging, holding, and resetting of the capacitor and the another capacitor for future phase differences detected by the phase frequency detector.